REPORT DOCUMENTATION PAGE

Form Approved
OMB No 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	May 25, 1995	Final Report 4/1/95 - 4/30/95

4. TITLE AND SUBTITLE

Novel Ferroelectric Heterostructures for High-Density DRAMS

5. FUNDING NUMBERS

DAAH04-94-C00021

6. AUTHOR(S)

Pang-Jen Kung, David B. Fenner

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Advanced Fuel Research, Inc.
87 Church Street
East Hartford, CT 06108

8. PERFORMING ORGANIZATION REPORT NUMBER

529025

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

U. S. Army Research Office
P. O. Box 12211
Research Triangle Park, NC 27709-2211

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

The view, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.

12a. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for Public release:
ABIR Report, distribution unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

In pursuit of oxide ferroelectric materials in perovskite phases with high dielectric constants used as storage capacitor dielectrics in new-generation dynamic random access memories (DRAMs), development of the process for fabricating film capacitors in planar structures of small dimensions is a central issue of great importance. From the point of view of device performance, such effort includes not only the deposition of epitaxial ferroelectric films but also the integration of associated top and bottom electrodes. The objective of the present study is, therefore, to explore the feasibility of a process based on all oxide materials for dielectrics and electrodes. As such, thin, epitaxial ferroelectric films (FE) including $BaTiO_3$, (Ba, Sr)TiO_3, and Pb(Zr, Ti)O_3 stacked in a multilayer structure of M/FE/M/B, where M is the conducting oxide electrode and B is the oxide buffer layer, have been successfully grown in this work by pulsed laser deposition on Si(100) wafers. Scanning electron microscopy, X-ray diffractometry, and transmission electron microscopy were employed to characterize these multilayer films for their morphology, crystallinity, and microstructure, respectively. Dielectric constants, leakage, hysteresis loops, remanent polarization, saturation voltage, and fatigue were measured to study the device potential. Our findings have provided valuable information on the realization of oxide ferroelectric film capacitors applied in DRAMs, but more work is still needed to improve the fatigue behavior and understand the microstructure-related device physics.

14. SUBJECT TERMS

ferroelectric films, pulsed laser deposition, leakage, hysteresis loops, dielectric constants, lead zirconate titanate, barium titanate, barium strontium titanate

15. NUMBER OF PAGES

23

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UL	UL	UL	UL

ADVANCED FUEL RESEARCH
P. O. Box 380379
East Hartford, Connecticut 06138-0379
Telephone (203) 528-9806
Fax (203) 528-0648

"Novel Ferroelectric Heterostructures for High-Density DRAMS"

PHASE I FINAL REPORT

Sponsored by
BMDO/DEPT OF THE ARMY
Small Business Innovation Research Program
Contract Number DAAH04-94-C-0021

Prepared by
Pang-Jen Kung, Principal Investigator
(Qi Li, Former Principal Investigator)
David B. Fenner, Program Manager

Advanced Fuel Research, Inc.
87 Church Street
East Hartford, Connecticut 06108
Tel: (203) 528-9806
Fax: (203) 528-0648

Original Contract Period: July 1, 1994 - December 31, 1994
Extended Performance Period: July 1, 1994 - April 30, 1995

May 25, 1995

Novel Ferroelectric Heterostructures for High-Density DRAMS

Pang-Jen Kung, Qi Li, and David B. Fenner
Advanced Fuel Research, Inc.
87 Church Street
East Hartford, CT 06108

Table of Contents

A. Project Summary

Ferroelectric films offer the potential for a variety of device applications such as dynamic random access memories (DRAMs), nonvolatile memories, electro-optic switches, visual displays, detectors, etc. In pursuit of oxide ferroelectric materials in perovskite phases used as storage capacitor dielectrics in new-generation dynamic random access memories (DRAMs), high dielectric constants and excellent insulating properties are required. Due to the downsizing trend, for practical applications, development of the process for fabricating film capacitors in planar structures of small dimensions is a central issue of great importance. From the point of view of device performance, such effort includes not only the deposition of epitaxial ferroelectric films but also the integration of associated top and bottom electrodes. The objective of the present study is, therefore, to explore the feasibility of a process based on all oxide materials for dielectrics and electrodes. As such, thin, epitaxial ferroelectric films (FE) including $BaTiO_3$ (BTO), (Ba, Sr)TiO_3 (BSTO), and Pb(Zr, Ti)O_3 (PZT) stacked in a multilayer structure of M/FE/M/B, where M is the conducting oxide electrode and B is the oxide buffer layer, have been successfully grown in this

work by pulsed laser deposition on Si(100) wafers. We have made most of our effort in studying the capacitors based on (Ba, Sr)TiO_3 because this thin-film material will show no fatigue feature caused by ferroelectric domain switching in the device operating temperature range when the Ba to Sr ratio is selected properly [1]. The Ba/Sr ratio is also known to affect the dielectric constants observed in the (Ba, Sr)TiO_3 compound [2].

In this program we have demonstrated the feasibility of integrating fully epitaxial ferroelectric thin-film heterostructures with semiconductor integrated circuit (I.C.) technology for DRAM applications. Scanning electron microscopy, X-ray diffractometry, and transmission electron microscopy were employed to characterize these multilayer films for their morphology, crystallinity, and microstructure, respectively. Dielectric constants, leakage, hysteresis loops, remanent polarization, saturation voltage, and fatigue were measured to study the device potential. Our findings have provided valuable information on the realization of oxide ferroelectric film capacitors applied in DRAMs, but more work is still needed to improve the fatigue behavior and understand the microstructure-related device physics.

B. Summary of Problems, Descriptions, and Task Objectives

To develop new-generation DRAMs, high capacitance in planar structures of small dimensions is necessary. The dielectric materials, such as SiO_2 and Si_3N_4, currently being used in the semiconductor industry have low dielectric constants which requires complicated vertical structures to obtain enough charge storage density. As the device dimension is shrunk to smaller than 0.5 mm, difficulties in device fabrication will arise. Therefore, the use of high dielectric constant materials to store a great amount of charge in small areas becomes inevitable. In this regard, thin, epitaxial ferroelectric films used as memory cells can offer several advantages including their switching voltages lower than those in conventional thick-film devices (and hence higher reliability) as well as high resistance to chemical and charge segregation.

In order for the use of DRAMs, leakage currents in the ferroelectric films have to be eliminated, and the fabrication process is expected to be integrated easily with existing silicon integrated circuit (I.C.) technologies. As a consequence, in addition to developing reproducible processes for the growth of high-quality ferroelectric films on common IC substrates of Si and GaAs, fabrication of the associated electrodes and their effects on overall capacitor performance also have to be taken into account. An improper electrode material can lead to interdiffusion, cracking, poor adhesion, fatigue-related degradation, polycrystalline films as deposited subsequently on its top, and so on. To grow an epitaxial ferroelectric film, the electrode material thus must be structurally compatible with the ferroelectric film. As long as oxide ferroelectric films are of interest, electrodes based on various oxide films, instead of widely used Pt or Al, seem to be the reasonable choice. As such, the processes for epitaxial growth of heterostructures consisting of a ferroelectric thin film sandwiched between two conductive oxide films on Si wafers first have to be explored before DRAM applications are pursued.

The objectives of this work are, therefore, to demonstrate: (i) the feasibility of depositing an epitaxial $La_{1-x}Sr_xCoO_3$ (LSCO) electrode on yttria-stabilized ZrO_2 (YSZ) buffered silicon

substrates; (ii) the feasibility of depositing multilayer, epitaxial $La_{1-x}Sr_xCoO_3/Ba_{1-y}Sr_yTiO_3/La_{1-x}Sr_xCoO_3$ (LSCO/BSTO/LSCO) heterostructures on YSZ-buffered Si substrates; (iii) the high performance of this simple metal-insulator-metal (MIM) capacitor device; and (iv) the compatibility of these devices with silicon ICs. These objectives will be met by accomplishing four tasks. First, we will deposit an epitaxial LSCO bottom electrode on YSZ-buffered Si substrates, and evaluate and improve the film quality. Second, we will deposit ferroelectric BSTO on top of the LSCO layer. Third, we will add another epitaxial LSCO layer on top of the ferroelectric film. Fourth, we will pattern the top LSCO electrode to form an MIM capacitor structure. The performance of this MIM capacitor will be fully evaluated. Note that during each of the deposition steps, film quality will have to be evaluated, and the deposition process is modified to optimize the film quality. The following milestones will be accomplished during this project:

- 1 - Epitaxial LSCO bottom electrode made on YSZ/Si(100)
- 2 - Epitaxial BSTO/LSCO achieved on YSZ/Si(100)
- 3 - Epitaxial LSCO/BSTO/LSCO achieved on YSZ/Si(100)
- 4 - Epitaxial MIM capacitor made on silicon wafer
- 5 - Initial evaluation of the integration of ferroelectric devices with Si circuitry made

C. General Methodology and Technical Background

C.1. Oxide Ferroelectric Films and Their Applications in High-Density DRAMs

The background for this work is in the following areas: (i) pulsed laser deposition (PLD) applied for epitaxial growth of oxide thin-film materials [3, 4], (ii) structural and electrical properties of epitaxial (La, Sr)CoO_3 films [5] - a new electrode material, (iii) ferroelectric M/FE/M capacitor structure [6], and (iv) ferroelectric device testing.

For years *AFR, Inc.* has made significant effort in applying PLD for the growth of high-temperature superconductors. The use of PLD to deposit perovskite ferroelectrics and conductive oxides is a natural extension to our previous research activities. A complete PLD system developed by *AFR, Inc.* is shown in Fig. 1, which has been utilized to grow epitaxial YBCO films on YSZ-buffered Si wafers on a daily basis.

The choice of LSCO as the electrode material in the present project is due to its low substrate temperature (600-675 °C) during deposition and low room-temperature resistivity, 90 ohms-cm, almost a factor of 3 lower than that of YBCO. To obtain good lattice match with many perovskite oxide ferroelectrics (cubic crystals with lattice constants around 0.4 nm), LSCO is an ideal candidate and in addition, it also exhibits excellent structural and electrical properties.

For thin-film capacitors applied in DRAMs, they must have high dielectric constants and large coercive field, but no spontaneous polarization. So far, (Ba, Sr)TiO_3 (BSTO) is known to be one of the most promising materials for the 256-Mb generation DRAMs. It belongs to the general class of ferroelectric materials based on the perovskite structure [7]. Since the Curie temperature of $BaTiO_3$ is about 120 °C, which decreases linearly with increasing Sr

concentration, the transition temperature and the pyroelectric coefficient in (Ba, Sr)TiO_3 can be tailored over a broad range [8, 9]. Moreover, its dielectric constant also depends on its grain size as shown in Fig. 2. Because of the difficulty in obtaining epitaxial film growth in this compound and its dielectric constants in bulk crystals currently known always higher than those in thin-film material, development of a deposition process for epitaxial BSTO films of high dielectric constants turns out to be very challenging. If achieved, this accomplishment will considerable enhance the capacitor performance and endurance [10, 11].

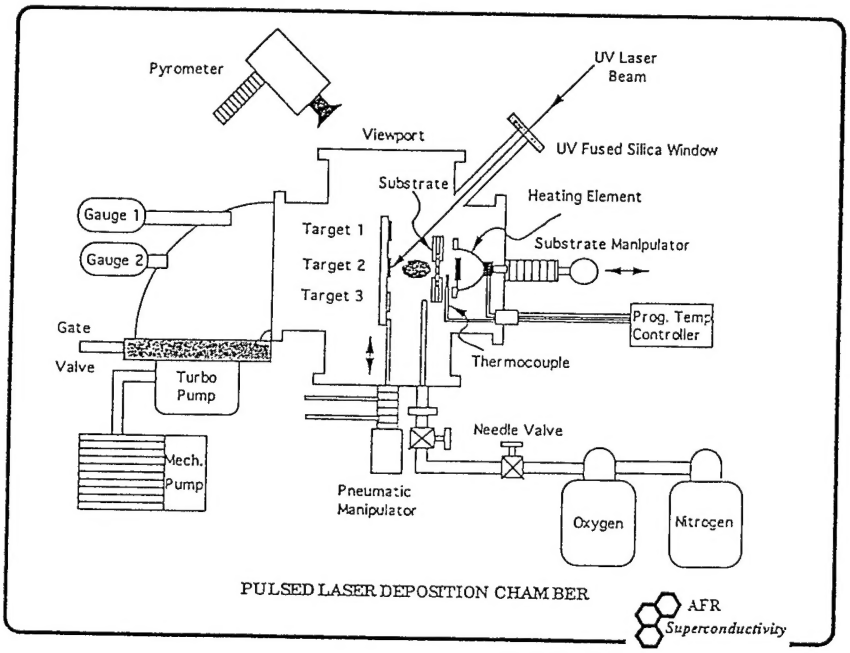

Figure 1. The pulsed laser deposition (PLD) system at *AFR, Inc.*

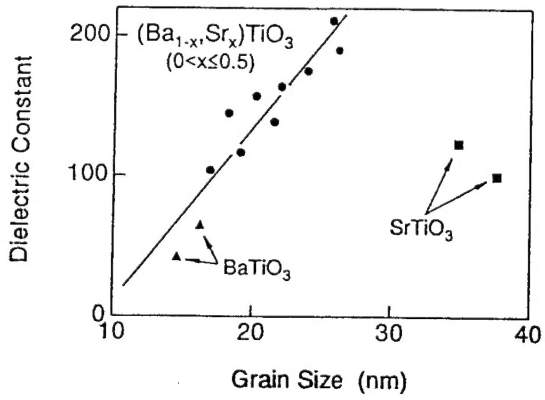

Figure 2. Relation between dielectric constant and mean grain size for the samples crystallized at 650 °C [2].

As oxide heterostructures are deposited, AFR, Inc. has full capabilities of fabricating hundreds of capacitors in a Si chip for device testing. Figure 3 shows sketches of a YBCO bolometer patterned from a YBCO film epitaxially grown on an epitaxial YSZ-buffered Si(100) wafer recently developed by *AFR* [12, 13]. The final capacitors will be tested for their dielectric constants, leakage, hysteresis loops, remanent polarization, saturation voltage, and fatigue behavior.

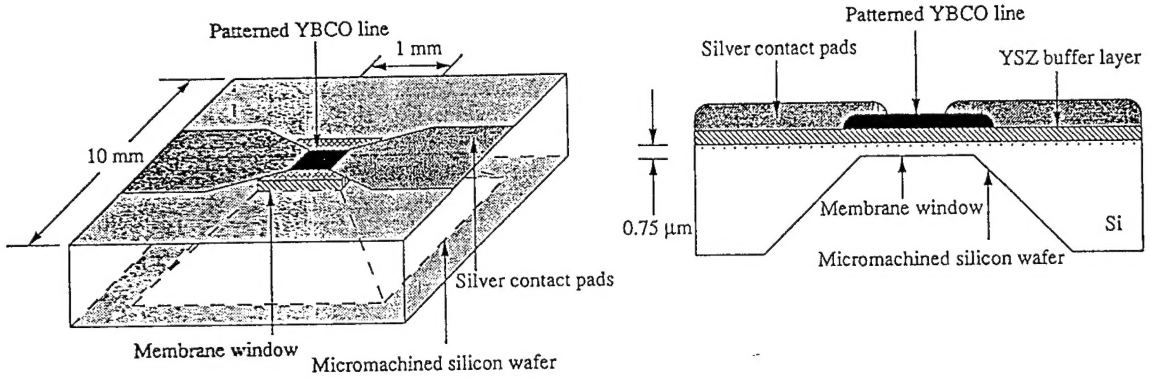

Figure 3. Sketches of a YBCO bolometer patterned from a YBCO film epitaxially grown on an epitaxial YSZ-buffered Si(100) wafer.

C.2. Previous Experience with Ferroelectric Materials at AFR, Inc.

Recently, *AFR. Inc.* have completed two SBIR Phase-I projects. The first one was funded by the *Department of Energy* under the Contract Number DE-FG05-93ER81591 to develop the technology for on-chip ferroelectric energy storage capacitors for Si solar cells. A single-layer epitaxial $BaTiO_3$ capacitor was fabricated to show an input/output current of 1 A/cm^2, three orders of magnitude higher than a typical thin-film lithium microbattery. The second project was supported by the *National Science Foundation* under the Contract Number: DMI-9361597. The objective of the NSF program was to develop ferroelectric material and advanced fabrication methods to produce the fastest and most sensitive room temperature infrared detectors available for arrays or single detector. A fully functional, uncooled pyroelectric detector based on either PZT or BTO films was fabricated and tested. The present program - *Oxide Ferroelectric Films and Their Applications in High-Density DRAMs,* therefore, can be viewed as the continuous effort made by *AFR, Inc.* in ferroelectrics research. We would like to see our relevant activities

and capabilities to be extended in the near future so that these prototype devices or systems realized and tested via the support from SBIR Phase I programs can be eventually developed into commercial products.

D. Technical Results

During the project performance period, we have fabricated 73 multilayer films; 35 made in July 1 - December 31, 1994 and 38 made in January 1 - April 30, 1995. Thin, epitaxial ferroelectric films (FE) including $BaTiO_3$, (Ba, Sr)TiO_3, and Pb(Zr, Ti)O_3 stacked in a multilayer structure of M/FE/M/B, where M is the conducting oxide electrode and B is the oxide buffer layer, as summarized in Fig. 4, have been grown by pulsed laser deposition (PLD) on Si(100) wafers that are typically 1 cm^2 and 15-16 mil thick.. Films were characterized by scanning electron microscopy (SEM), X-ray diffractometry (XRD), and transmission electron microscopy (TEM) for their morphology, crystallinity, and microstructure, respectively. Resistance curves as a function of temperature. R(T), were measured which was used as a routine method to examine the film quality as the films were deposited prior to further processing. An RT66A standardized ferroelectric test system (*Radiant Technologies, Inc.*) was employed to perform the measurements of dielectric constants, leakage, hysteresis loops, remanent polarization, saturation voltage, and fatigue behavior, with several different electrode configurations being explored.

D.1. Task 1 - Deposit Conductive Oxide Bottom Electrode on Si

Before depositing ferroelectric materials for thin-film capacitors, the first step is to prepare a high-quality conductive bottom electrode that will help the epitaxial growth of other layers deposited on its top. To provide a good lattice match between neighboring layers and to avoid the leakage potentially through Si substrates, an epitaxial Y_2O_3 stabilized ZrO_2 (YSZ) film was first grown on Si(100) wafers prior to the deposition of other oxide films. As shown in Fig. 5, YBCO films with a superconducting width, ΔT, less than 1.5 K are obtained on YSZ-buffered Si(100) substrates. The key to successful YSZ deposition is that the Si wafer surface is terminated by hydrogen which is a spin-etch process developed by D.B. Fenner (program manager of this project) a few years ago. In the present study, we have found that a thin (10-15 nm) YBCO film can serve as the template layer for subsequent growth of the epitaxial (La, Sr)CoO_3 (LSCO) film. Without high-quality YBCO films in place, conductive LSCO films can act semiconductor-like even as deposited, they have very smooth surfaces and show right film color. In general, for R(T) measurements, epitaxial LSCO films should follow the metallic behavior in the temperature range of 150-300 K. We have demonstrated in the present program that epitaxial LSCO films can be routinely deposited at substrate temperature below 700 °C under a 200 mTorr oxygen environment. As a member in the perovskite family, the oxygen content in LSCO is expected to affect to some degree its electrical properties. In other words, the slope of a R(T) curve can be changed exclusively due to such an effect. When this is the case, based on our experience with YBCO films (another perovskite member), cooling process after deposition can be very crucial in tailoring the electrical properties of LSCO films. But we have not yet had opportunities to investigate it in details.

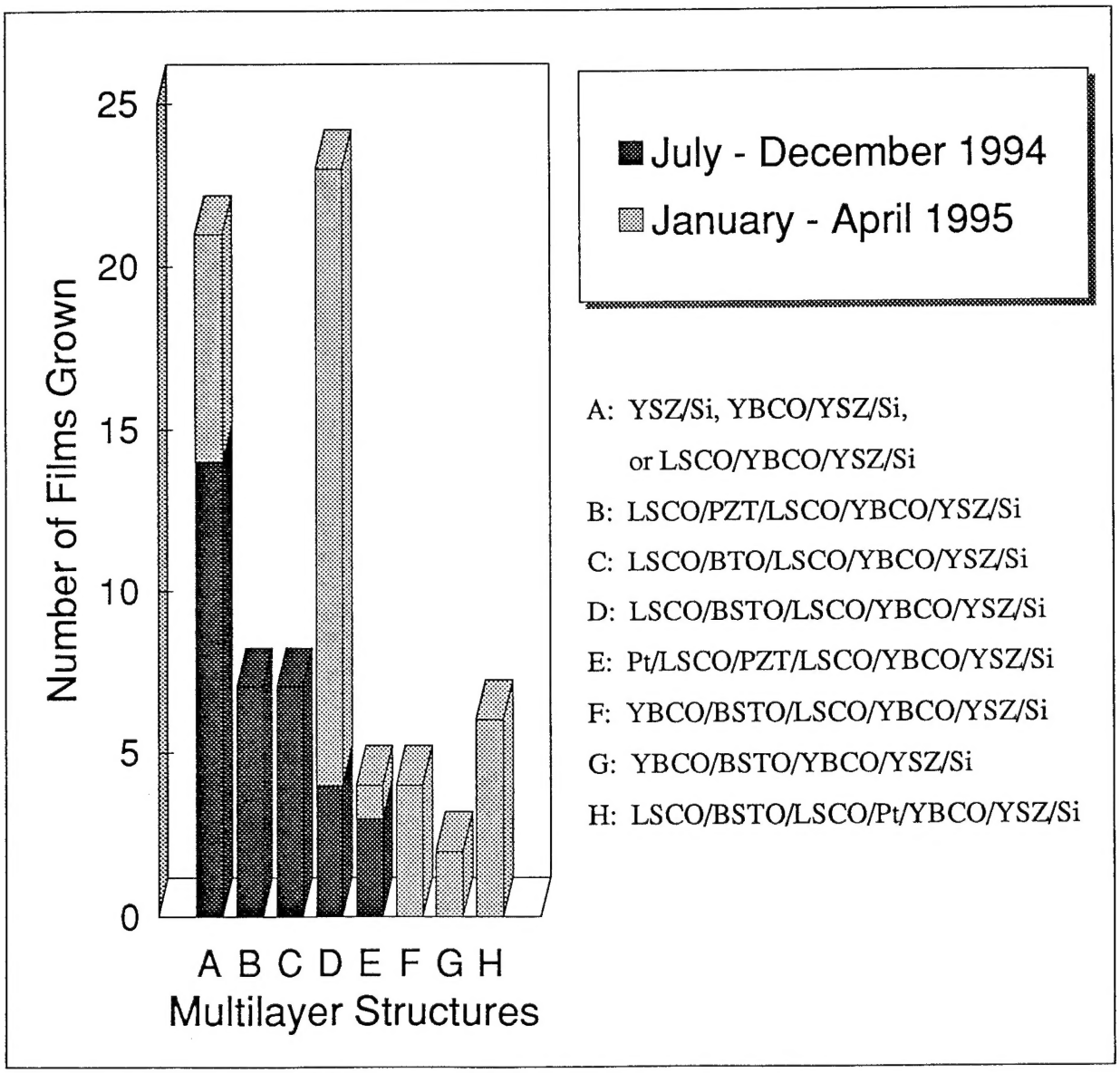

Figure 4. A summary of the various stacking structures of thin ferroelectric films fabricated during the project performance period.

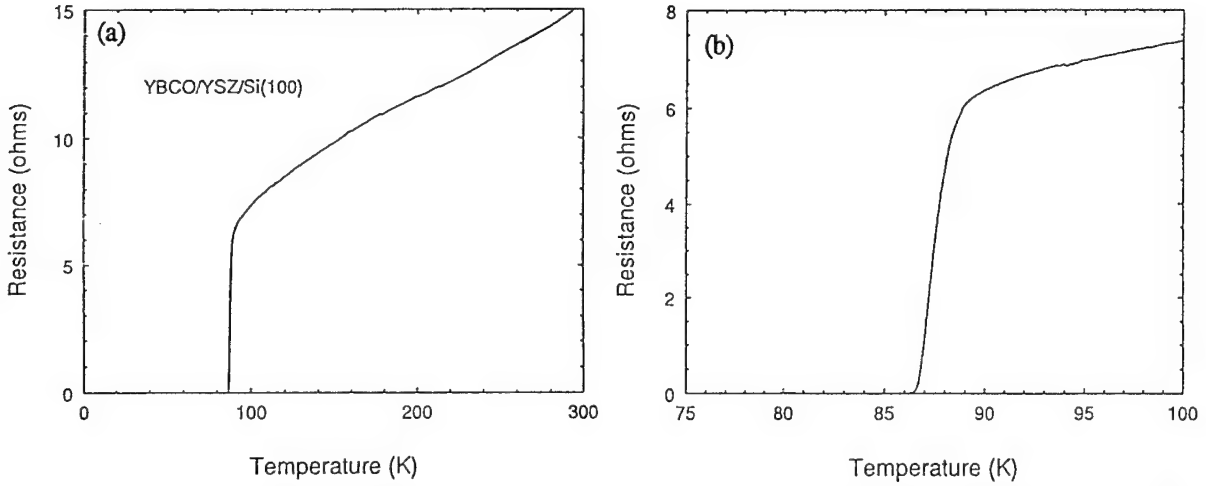

Figure 5. Temperature-dependent resistance measured on a YBCO film deposited on YSZ-buffered Si(100) substrates in which (b) is plotted in the temperature range of 75-100 K of the R(T) curve shown in (a).

D.2. Task 2 - Deposit a Ferroelectric Film on LSCO Layer

Ferroelectric films such as Pb(Zr, Ti)O_3 (PZT), $BaTiO_3$ (BTO), and (Ba, Sr)TiO_3 (BSTO) were deposited on top of the LSCO layer by PLD at several different substrate temperatures. The work was mainly focused on (Ba, Sr)TiO_3, and Pb(Zr, Ti)O_3 and $BaTiO_3$ both were studied only for comparison. The corresponding best substrate temperatures for epitaxial growth are around 700 °C, 630 °C, and 750 °C, as suggested by X-ray diffractometry (XRD) analyses. Figure 6 shows XRD patterns for the (Ba, Sr)TiO_3 films deposited at 700 °C and 750 °C. As the substrate temperature is higher than 720-730 °C, the XRD peaks due to orientations other than <001> are getting stronger, which implies a gradual loss of epitaxial quality in the films. For most of (Ba, Sr)TiO_3 films prepared here, their thickness is somewhere around 80-90 nm.

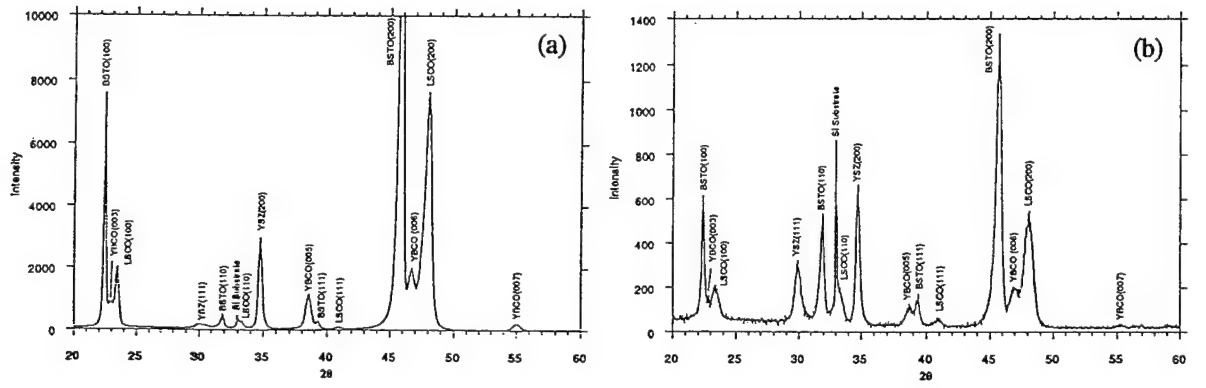

Figure 6. XRD patterns for the (Ba, Sr)TiO_3 films deposited at the substrate temperature of (a) 700 °C and (b) 750 °C.

D.3. Task 3 - Deposit LSCO Top Electrode

As illustrated in Fig. 4, fifty two multilayer films of M/FE/M/B on Si(100) with a (La, Sr)CoO_3 top electrode deposited have been prepared in this work. Temperature-dependent resistance curves, R(T), were measured on these films using a standard four-probe method. With four Ag contacts made across individual deposited layers at four corners of a Si chip (see Fig. 7), the film conductivity can be examined, in particular, for the top LSCO electrode layer. Here, depending on how Ag dots actually contact individual layers, we may obtain a net R(T) curve obtained from the superposition of resistance contributed by each oxide layer, which also allows us to measure the superconductivity of the underlying YBCO layer. As mentioned earlier, epitaxial LSCO films should exhibit the metallic behavior in 150-300 K. It is probably true that in many cases, if the top LSCO layer does not show a proper R(T) curve, the rest layers in the film will not be characteristic of epitaxy. Figures 8 (a) and (c) show the R(T) curves of the films corresponding to the same ones for XRD analysis in Figs. 6 (a) and (b). It is obvious that the resistance of the film of poor epitaxy increases rapidly with decreasing temperature. $T_{c,\,onset}$ of the YBCO layer in Fig. 8 (a) is 88 K. Notice that in Fig. 8 (b), R(T) values do increase slowly as the temperature is decreased; however, the XRD pattern obtained from this film, which was deposited under the same conditions as those for Fig. 8 (a), is similar to that shown in Fig. 6 (a). This suggests that (i) XRD results do not reflect on a reliable basis the electrical properties associated with films and (ii) the mechanism (e.g., the difference in the oxygen content between films) to cause this inconsistency requires further investigation. Overall, it may be fair to say that for the films with reasonable quality, their R(T) curves do not increase tremendously with decreasing temperature.

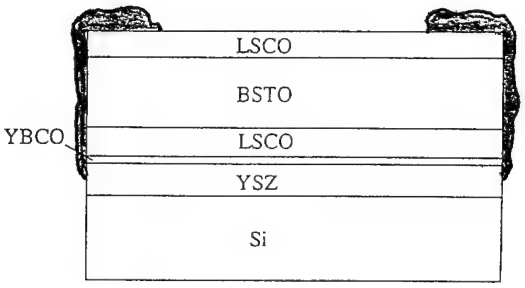

Figure 7. The configuration of four Ag contacts painted on an as-deposited multilayer film on a Si chip for R(T) measurements using a standard four-probe method.

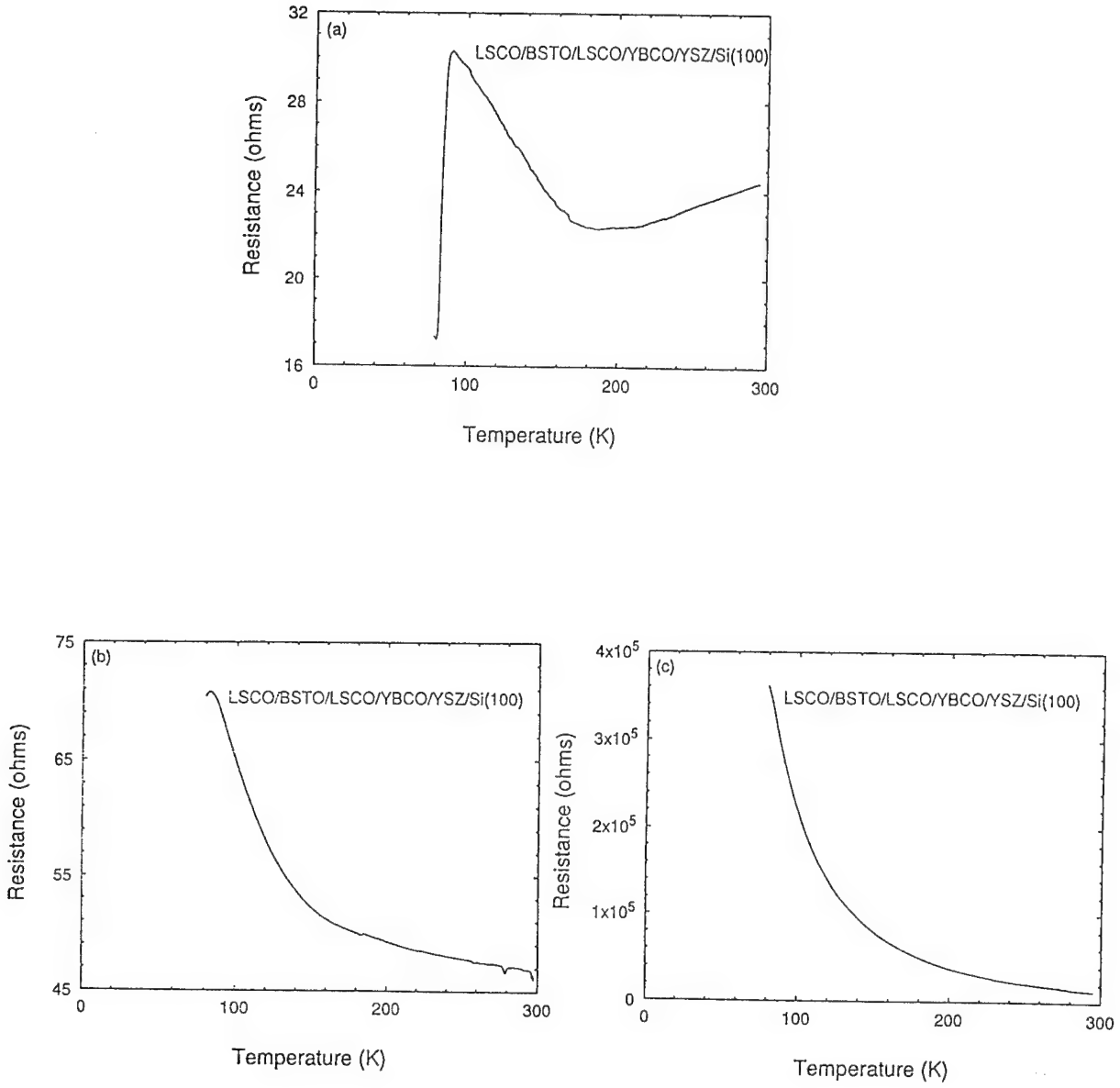

Figure 8. R(T) curves obtained from the films with their ferroelectric layer deposited at (a) and (b) 700 °C and (c) 750 °C.

In addition to LSCO, we have also deposited multilayer films with YBCO for top and bottom electrodes as well as LSCO for bottom electrode and YBCO for top electrode. The former case seems to show reasonable results in terms of the R(T) characteristics of the film, but it is not as good as the ones using LSCO for top and bottom electrodes. The latter, on the other hand, always exhibits a semiconductor-like R(T) curve, which can be due to the interdiffusion related to the LSCO bottom layer or the ferroelectric layer occurring during the deposition of top

YBCO layer. Typically, YBCO is grown at the temperature of about 100 °C higher than that for these two oxide materials. This observation implies the importance of the arrangement of deposition sequences and the choice of materials in growing multilayer films.

To study the microstructure of the multilayer films, an as-deposited film exhibiting its R(T) curve of the metallic behavior with 4-point resistance values lower than 30 ohms in 0-300 K was cut, ground, dimpled, and milled for cross-sectional transmission electron microscopy (TEM) analysis. The purpose of the analysis was to determine the (I) thickness of each layer in the film, (ii) crystal structures of individual layers, and (iii) crystallographic relationship between the layers and the substrate. Figure 9 illustrates a high magnification image of the film, in which the individual layers were estimated to have the following thickness: layer 1 (YSZ) 45 nm, layer 2 (YBCO) 16 nm, layer 3 (LSCO) 33 nm, layer 4 (BSTO) 80 nm, and layer 5 (LSCO) 40 nm. The corresponding electron diffraction patterns including the Si substrate are shown in Fig. 10. These results indicate that:

- The YSZ layer is formed with a cube-to-cube relationship with the Si(100) substrate. The interface between YSZ and Si is free from any secondary phases which suggests that our spin-etch process used for Si wafer cleaning effectively removes SiO_2 from Si wafers to facilitate the epitaxial growth of YSZ.
- The 2nd and 3rd layers appear to be microcrystalline with a crystallite size of less than 5 nm which gives rise to a ring pattern.
- The 5th layer shows an identical diffraction pattern, including orientation, as the 4th layer. Both of them exhibit a cubic crystal structure. Perfect epitaxy between these two layers is evidenced in a much higher magnification image of the film (not shown here) by the continuity of lattice fringes across these layers.

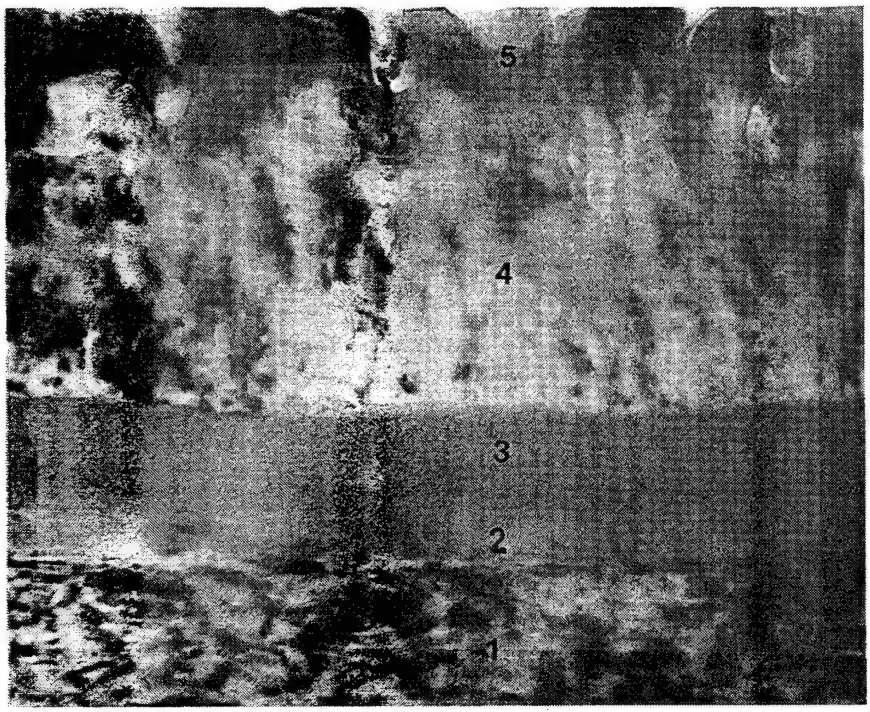

Figure 9. A high magnification, cross-sectional image of the film of LSCO/BSTO/LSCO/YBCO /YSZ on Si(100) substrate.

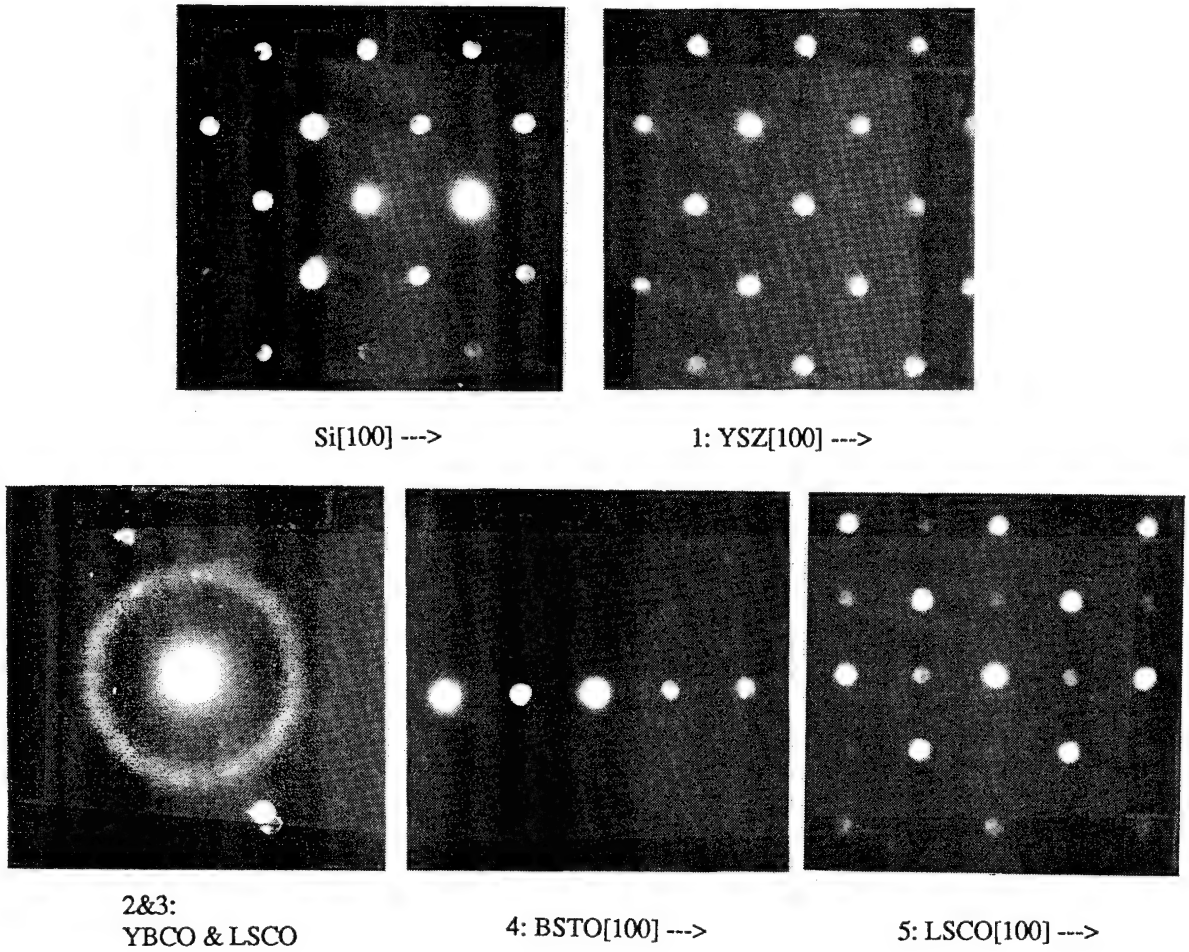

Figure 10. Electron diffraction patterns corresponding to the individual layers as shown in Fig. 9.

D.4. Task 4 - Fabricate and Test the M/FE/M Capacitor Structure

For those films showing epitaxy and desired R(T) characteristics, they were patterned photolithographically to form many isolated top electrodes of small dimensions in the order of μm. The patterns for round and square electrodes used for the measurements of ferroelectric properties are shown in Fig. 11. With the aid from microfabrication techniques, hundreds of capacitors can be obtained in a 100-mm^2 Si chip. In several cases, top electrodes with the underneath ferroelectric layer were also fabricated during deposition by using a Si shadow mask with 2 x 2 mm^2 micromachined windows. Figure 12 summarizes three different probing configurations adopted in the present work; namely, (1) dot-to-dot, formed by acid wet etching, in the top electrode layer, (2) dot in the top electrode layer to the bottom electrode (Au pads were deposited for making better contact), and (3) top electrodes formed via a shadow mask to the bottom electrode. Ferroelectric tests were performed by driving one electrode and measuring the return at another electrode in the array; both adjacent and non-adjacent electrodes. Based on the measurements, we have observed:

- For films with the thickness of BSTO ferroelectric (FE) layer less than 100-nm, they behave leaky at test voltages above 1-2 volts; however, leakage can be improved with increasing FE thickness. We are able to test the devices with a 180-nm thick FE layer at up to 20 volts before resistive leakage becomes dominant. In general, the smaller devices appear to be less leaky than the larger ones.
- Most of LSCO/BSTO/LSCO/YBCO/YSZ capacitors exhibit dielectric constants in the range of 50-150.
- In preliminary study for comparison, PZT seems to show the values of saturation polarization higher than BTO and BSTO at the same maximum applied voltage (see Fig. 13); however, details on the difference in other ferroelectric parameters and its correlation with microstructures require further investigation. Fatigue testing of the heterostructures based on PZT carried out at 10 kHz in an a.c. applied field of 2 volts is shown in Fig. 14.
- The remanence ΔP in the pulsed measurement is not significant, typically around 0.5 $\mu C/cm^2$. What causes such low ΔP values is not clear at the moment.

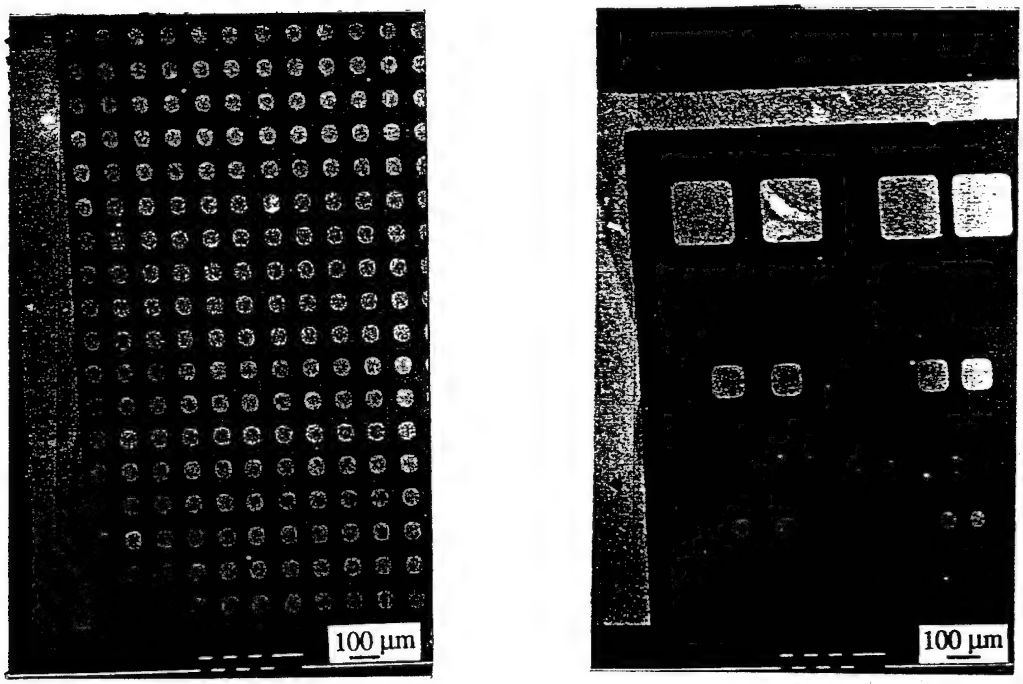

Figure 11. The patterns for round and square electrodes used for the measurements of ferroelectric properties.

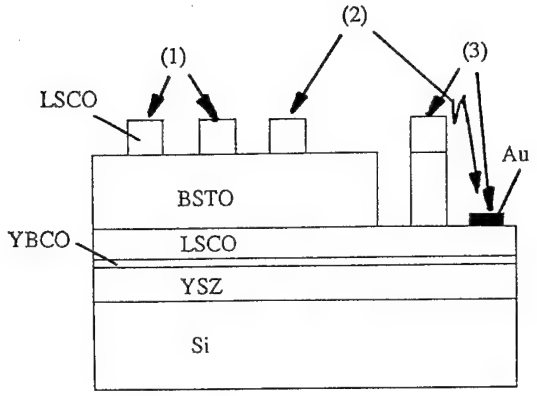

Figure 12. Three different probing configurations adopted in the present study.

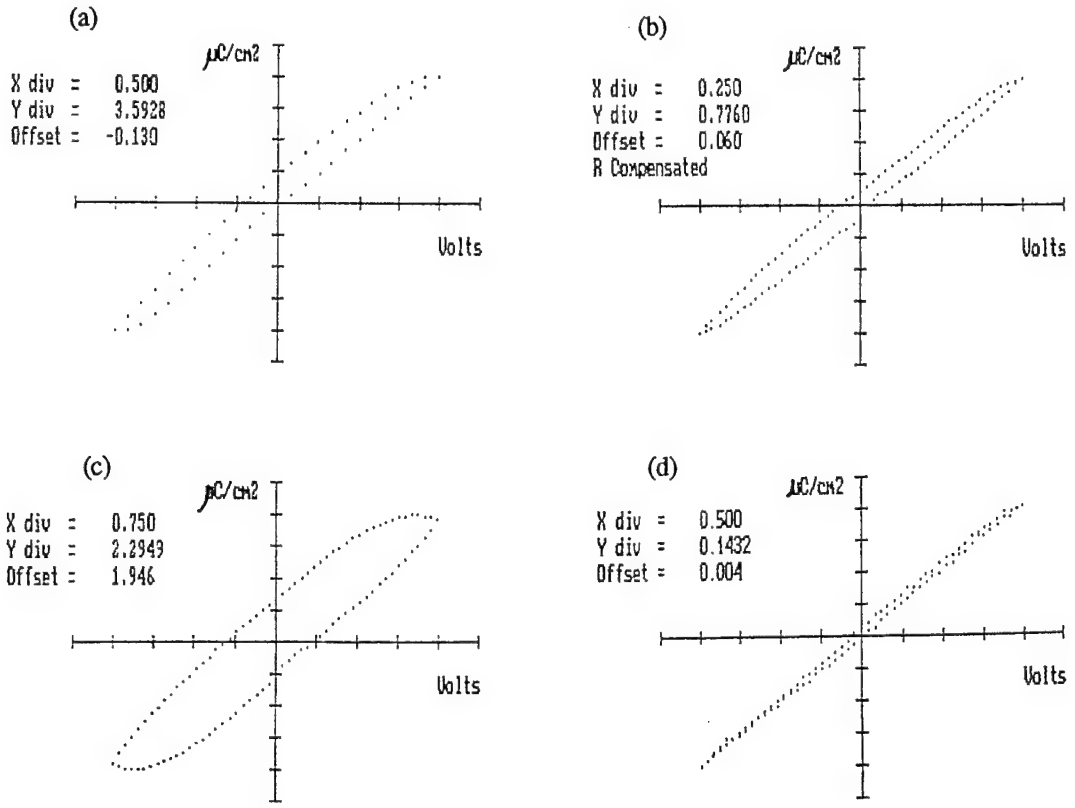

Figure 13. A comparison in the hysteresis loops among the ferroelectric films deposited under similar conditions for (a) PZT, (b) and (c) BTO, and (d) BSTO.

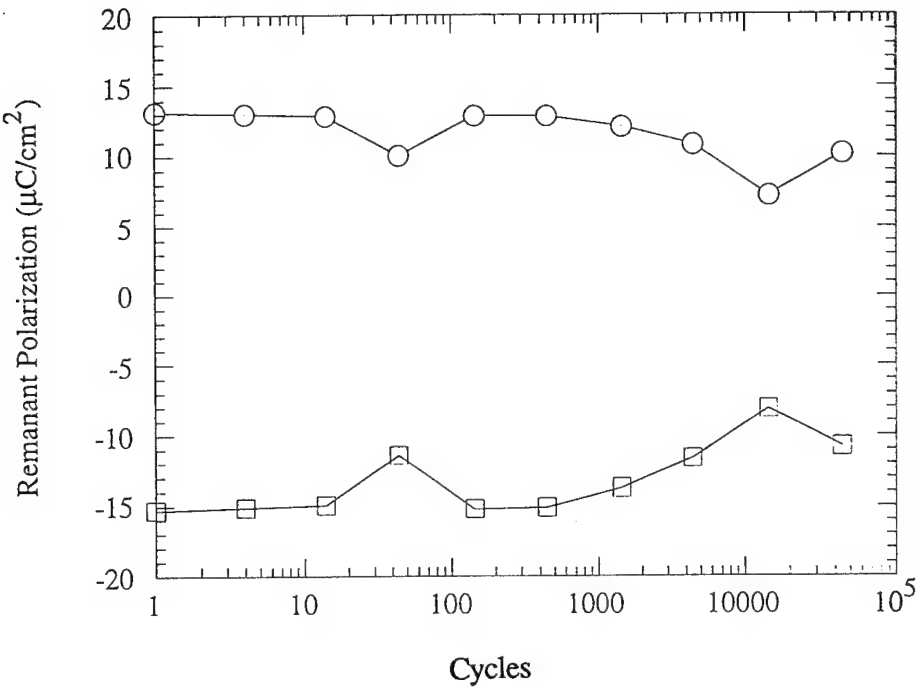

Figure 14. The fatigue curve obtained from a capacitor of LSCO/PZT/LSCO/YBCO/YSZ on Si.

To eliminate leakage and to improve the fatigue behavior in our BSTO ferroelectric films, we then replaced LSCO top and bottom electrodes with LSCO/Pt hybrid electrodes as illustrated in Fig. 15, where Pt thickness is less than 10 nm. Notice that a change like Fig. 15 (b) can probably affect the overall film epitaxy (due to YBCO not serving as a template layer for LSCO) and hence R(T) curves and other properties. To clarify these concerns, XRD patterns (see Fig. 16) were recorded before and after the deposition of BSTO layer. Apparently, although we still maintain reasonable epitaxy in our films, the peaks due to LSCO are shifted towards the low-angle side. The peaks due to Pt(111) at 39.7° and Pt(200) at 46.2°, which are very close to the positions for LSCO(111) and LSCO(200), respectively, are not shown here. It has been thought that perhaps Pt and LSCO form other compounds at the interface, leading to both the shift in peak positions and the change in peak widths. It also surprises us that the BSTO layer grown on top of the LSCO layer still keeps its <100> orientation. Typical R(T) curves measured on the capacitor structure as illustrated in Fig. 15 (b) are shown in Fig. 17, in which (a) and (b) are obtained for Pt deposited at 500-550 °C and (c) is for Pt at 100-120 °C. So far, with the use of hybrid electrodes as shown in Fig. 15 (a), ferroelectric properties seem not to be affected significantly. However, a configuration in Fig. 15 (b) does increase the dielectric constant from 68 obtained in a capacitor with LSCO electrodes to 376. The difference in hysteresis loops is clearly seen in Fig. 18. But, unfortunately, leakage still exists in the capacitors with hybrid electrodes, and their remanent polarization also needs to be further improved.

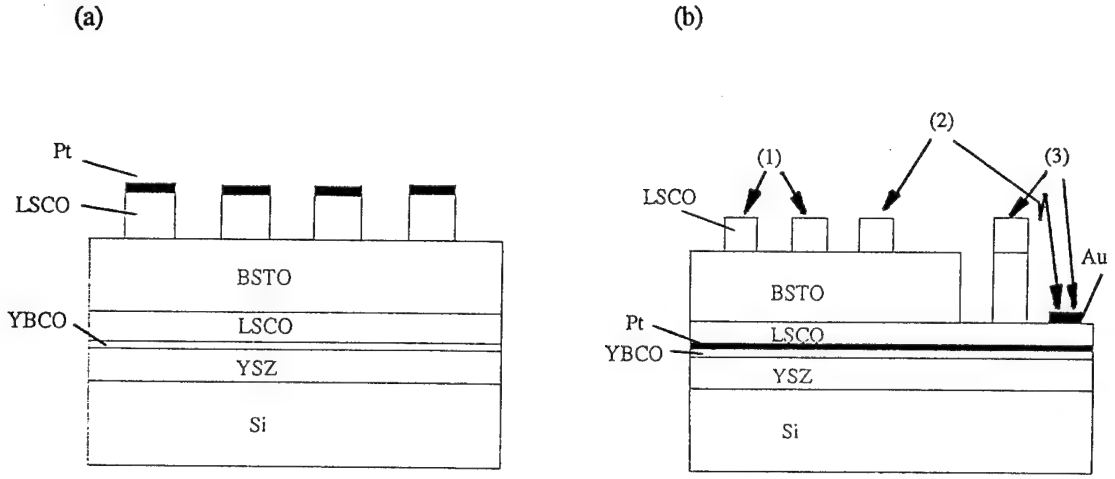

Figure 15. Two types of hybrid electrodes for thin-film capacitors.

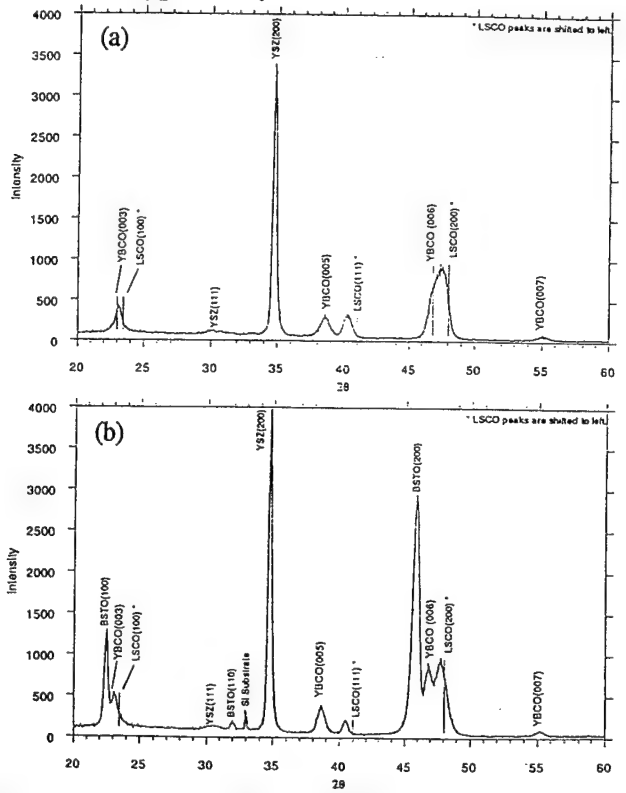

Figure 16. XRD patterns for the film with a LSCO/Pt bottom electrode recorded (a) before and (b) after the deposition of BSTO layer.

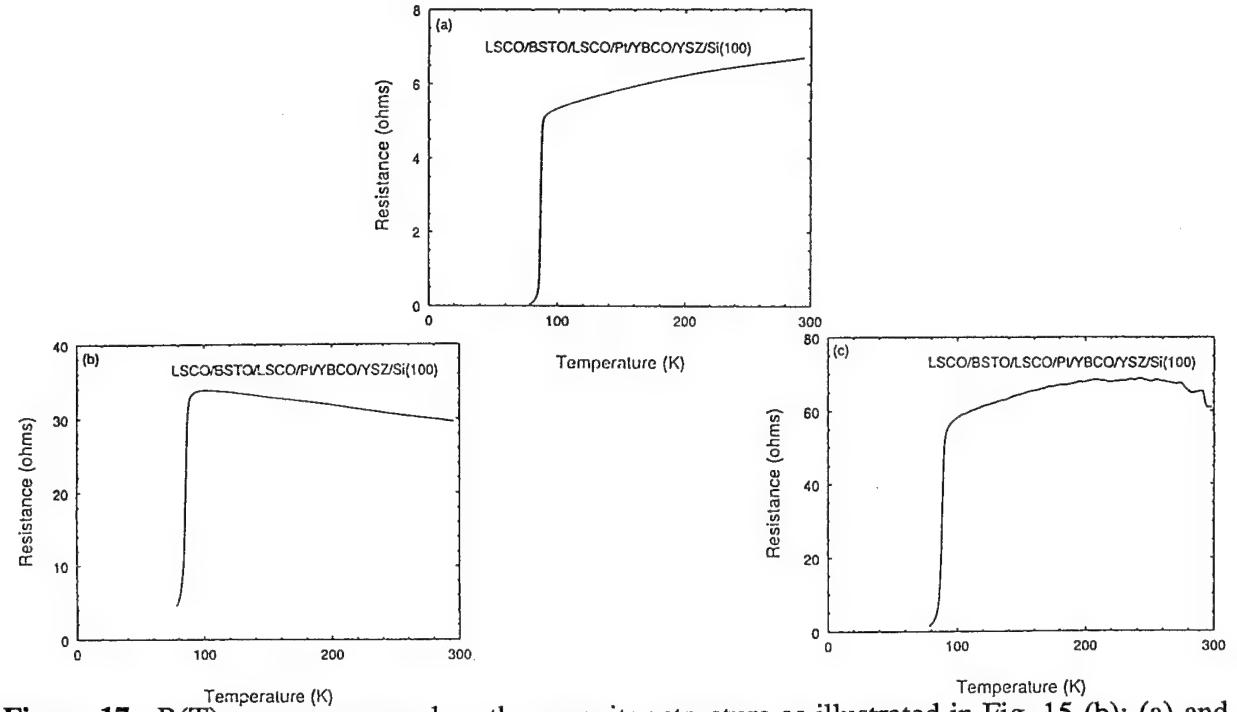

Figure 17. R(T) curves measured on the capacitor structure as illustrated in Fig. 15 (b); (a) and (b) are obtained for Pt deposited at 500-550 °C and (c) is for Pt at 100-120 °C.

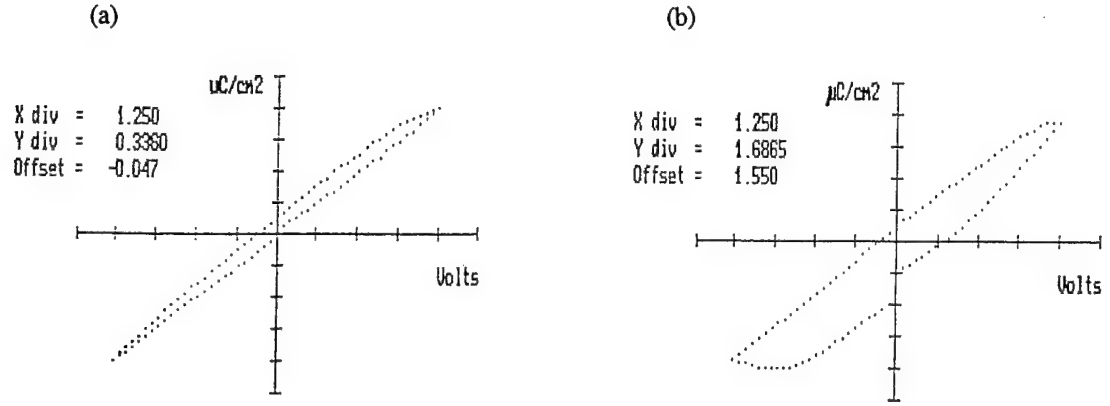

Figure 18. Hysteresis loops measured on the films prepared under the same growth conditions with a bottom electrode of (a) LSCO and (b) LSCO/Pt.

E. Important Findings and Conclusions

This Phase-I program has been designated to demonstrate the feasibility of fabricating thin-film capacitors on silicon wafers for high-density DRAMs based on all thin-film oxides for dielectrics and electrode materials, namely M/FE/M/T/B, where

M: top and bottom (La, Sr)CoO_3 electrodes, 30-40 nm
FE: (Ba, Sr)TiO_3 ferroelectrics, 80-180 nm
T: $YBa_2Cu_3O_7$ template layer, 10-20 nm
B: Y_2O_3 stabilized ZrO_2 buffer layer, 40-50 nm

Our experimental results have indicated that such a concept, as described in our Phase-I proposal, is a promising approach. We are able to achieve epitaxial growth, as evidenced by XRD and TEM analyses, for each oxide layer deposited on Si(100) wafers, which is encouraging in the sense of integrating the heterostructures developed here with existing silicon I.C. technologies. However, as compared with bulk oxide ferroelectrics and the thick films prepared by a sol-gel process, our thin-film capacitors appear to be more leaky and show less remanent polarization. According to our findings, leakage obviously depends on the thickness of ferroelectric layer, and when the thickness is less than 100 nm, leakage becomes significant even with an applied voltage of 1-2 volts. The possible solutions to this problem can be either to grow thicker films or to use hybrid electrodes. The former case has been demonstrated in this work, whereas with only several heterostructures with hybrid electrodes having been prepared, it is not sufficient to draw any conclusion on the latter approach. But we do find that the application of hybrid electrodes in heterostructures improves significantly the dielectric constants (e.g., from 68 changed to 376) of the film capacitors. This is very important for high-density DRAM applications, in contrast to the case that the reversal polarization characteristics of ferroelectrics appear to be more critical (than high dielectric constants) while applied in nonvolatile memories.

We have found that R(T) curves for epitaxial (La, Sr)CoO_3 films should exhibit the metallic behavior. In many cases, even XRD analysis shows a preferred <100> (*c*-axis or *a*-axis) orientation in the films, it does not ensure a metallic R(T) curve to be obtained. But when the peaks due to <110> or <111> become significant, the resistance values do increase rapidly with decreasing temperature, implying that poor ferroelectric properties are likely resulted. In the present study, because of the limited time and funding, we do not investigate how the *c/a* ratio is varied by chemical compositions and deposition conditions. Such variations can cause severe fatigue and microcracking [14]. In general, high-resolution TEM or comprehensive analysis on XRD patterns via a Gaussian-squared method [15] is employed to probe *c/a* ratios and crystal strain induced during film growth. With detailed investigations conducted on microstructural analysis, the underlying mechanisms to cause the poor capacitor behavior can be understood, and this, in turn, leads to the activities to improve device performance in a more efficient way. In the case of hybrid electrodes applied in heterostructures, the study on the interface properties and potential interdiffusion due to high substrate temperature also rely on microstructural analyses. As pointed out in the previous section, the $YBa_2Cu_3O_7$ and bottom (La, Sr)CoO_3 layers appear to be microcrystalline. Since both the bottom and top (La, Sr)CoO_3 layers were deposited under the same growth conditions, why there exists the difference in their crystallite sizes is not clear at the moment. In addition, how this affects the functions of an electrode in capacitors can be a key factor to device performance.

F. Implications for Future Research

As concluded from our effort made so far to study the feasibility of applying oxide ferroelectric heterostructures for high-density DRAMS, it clearly indicates that several research areas are well worth exploring further:

1. The effect of Ba/Sr ratios in (Ba, Sr)TiO_3 on the crystallite sizes and the degree of epitaxy in as-deposited films, and hence the resulting ferroelectric characteristics; how in-plane misorientation is related to device behavior.

2. How the actual oxygen content, perhaps being tailored by the cooling process after the film is deposited, in (La, Sr)CoO_3 films affects their overall electrical characteristics in terms of their role as the electrode material for thin-film capacitors.

3. Details on the relationship between microstructures, for instance, granular versus columnar features, and conduction mechanisms (e.g., space-charge-limited model, Schottky emission behavior, etc.) in ferroelectric films.

4. Approach to reducing leakage currents and improving dielectric constants and remanent polarization.

5. *In-situ* diagnosis of PLD during film growth for optimizing deposition parameters in order to establish a very reproducible fabrication process suitable for mass production in the future.

6. Development of fabrication technologies for large-area Si wafers (at least 2 inches) and reliable post-processing methods for patterning oxide heterostructures lithographically to manufacture thousands of tiny capacitors in Si chips.

It is our belief that the results obtained from the present Phase-I program have shown great potential for oxide ferroelectrics applied in high-density DRAMs. If a future Phase-II program could be funded, technical breakthroughs in the research areas as described above can be expected. Meanwhile, with the support from *AFR, Inc.*, we will continue part of our Phase-I research activities in oxide ferroelectrics.

G. Special Comments

G.1. Publications Planned

Two technical papers based on the results described above will be submitted in June for publication:

- P.J. Kung, Q. Li, and D.B. Fenner, "Epitaxial Growth of Ferroelectric Thin-Film Heterostructures with Oxide Electrodes on Silicon by Pulsed Laser Deposition," to be submitted to *J. Physics D: Appl. Phys.*

• P.J. Kung and D.B. Fenner, "Structural and Electrical Properties of Epitaxial $La_{0.5}Sr_{0.5}CoO_3/Ba_{0.4}Sr_{0.6}TiO_3/La_{0.5}Sr_{0.5}CoO_3$ Thin-Film Capacitors on Silicon," to be submitted to *Thin Solid Films*.

G.2. Professional Personnel

The *Electronic Materials and Devices Group* at *AFR, Inc.*, which is managed by the Program Manager (D.B. Fenner) on this contract, presently has in progress several SBIR contracts in the areas of high-temperature superconductive devices, *in-situ* diagnosis of pulsed laser deposition, and oxide ferroelectrics. This group has 4 principal staff members and 2 support staff members as listed below:

Principal Staff

David B. Fenner, Senior Physicist and Group Manager
Ph.D. in Physics, Washington University, 1976; over 80 publications, many in high-temperature superconductivity and infrared detectors.

Pang-Jen Kung, Senior Scientist
Ph.D. in Materials Science and Engineering, Carnegie Mellon University, 1993; over 35 publications in bulk and thin-film oxide superconductors, diamond films and applications, microstructural analysis, microelectronic devices, digital signal processing and biomagnetometry.

Peter Rosenthal, Senior Physicist
Ph.D. in physics, Stanford University, 1992; over 25 publications, many in high temperature superconductivity and Josephson junctions.

Joseph E. Cosgrove, Laboratory Manager
B.S. in Chemistry, University of New Haven, 1987.

Support Staff

Peter R. Solomon, President and Founder (in 1980) of *AFR, Inc.*
Ph.D. in physics, Columbia University, 1965; over 130 publications and reports.

David G. Hamblen, Vice President and Co-Founder of *AFR, Inc.*
Ph.D. in physics, University of Illinois, 1969; over 30 publications and reports.

H. Footnotes to the Text

1. T. Horikawa, N. Mikami, T. Makita, J. Tanimura, M. Kataoka, K. Sato, and M. Nunoshita, Jpn. J. Appl. Phys. **32**, 4126 (1993).
2. H. Kawano, K. Morii, and Y. Nakayama, J. Appl. Phys. **73**, 5141 (1993).
3. R. Ramesh, A. Inam, W.K. Chan, B. Wilkens, K. Myers, K. Remschnig, D.L. Hart, and J.M. Tarascon, Science **252**, 944 (1991).
4. J.S. Horwitz, K.S. Grabowski, D.B. Chrisey, and R.E. Leuchtner, Appl. Phys. Lett. **59**, 1565 (1991).

5. J.T. Cheung, P.E.D. Morgan, D.H. Lowndes, X.-Y. Zheng, and J. Breen, Appl. Phys. Lett. **62**, 2045 (1993).
6. Z.Q. Shi, Q.X. Jia, and W.A. Anderson, J. Electro. Mater. **20**, 939 (1991).
7. F. Galasso, "*Perovskite and High-T_c Superconductors*," Gordon and Breach, 1990.
8. V. Mehrotra, S. Kaplan, A.J. Sievers, and E.P. Giannelis, J. Mater. Res. **8**, 1209 (1993).
9. F. Jona and G. Shirane, "*Ferroelectric Crystals*," Pergamon, New York, 1962.
10. D.P. Vijay and S.B. Desu, J. Electrochem. Soc. **140**, 2640 (1993).
11. R. Ramesh, T. Sands, and V.G. Keramidas, Appl. Phys. Lett. **63**, 731 (1993).
12. D.B. Fenner (P.I.), Dept. of Energy, SBIR Phase II, Contract Number DE-FG01-90-ER81084.
13. D.B. Fenner (P.I.), Dept. of Defense, Contract Number DASG60-92-C-0115.
14. L.H. Parker and A.F. Tasch, IEE Circuits & Device Mag. **6**, 17 (1990).
15. P.J. Kung, E.J. Peterson, E.R. Flynn, C.B. Mombourquette, S.R. Foltyn, and R.J. Brainard, Physica C **224**, 58 (1994).

FISCAL REPORT

ADVANCED FUEL RESEARCH, INC.
87 Church Street
East Hartford, CT 06108

Report Date: May 22, 1995

Contract No. DAAH04-94-C-0021

Reporting Period: April 1 - April 30, 1995

	Contract Total		Prior Period Expeditures		Reporting Period Expeditures		Cummulative to Date Expeditures		Remaining Expenditures Per Contract	
	HOURS	COST	HOURS	COST	HOURS	COST	HOURS	COST	HOURS	COST
WAGES/SALARIES										
Senior Engineer	100		32		2		34		66	
Engineer	350		606		29		635		(285)	
Research Asst	385		4		0		4		381	
TOTAL LABOR	835	20,437	642	18,107	31	1,000	673	19,107	162	1,330
LABOR OVERHEAD		25,485		22,579		1,247		23,826		1,659
Materials		2,000		2,069		0		2,069		(69)
Subcontracts(0-25,000)				0		0		0		0
Travel				0		0		0		0
Consultants			0.00	0	0.00	0	0.00	0	0.00	0
Other Direct								0		0
G&A Base		47,922		42,755		2,247		45,002		2,920
G&A		7,380		6,584		346		6,930		450
Large Subcontracts	0	0					0.00	0	0.00	0
Subcontract Admin.		0		0		0		0		0
Total Costs		55,302		49,340		2,593		51,933		3,369
Fee (percent)		2,784		2,484		131		2,615		169
TOTAL COST + FEE	835	58,086	642.00	51,824	31.00	2,724	673.00	54,548	162.00	3,538

Pang-Jen Kung, Principal Investigator